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(C. McCreight)

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## CRYOGENIC SWITCHED MOSFET CHARACTERIZATION

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FOREWORD

This test report on cryogenic switched MOSFET characteristics covers the results of, and completes, Aerojet ElectroSystems Company efforts in accordance with Purchase Order A 80598B (JMM) from Ames Research Center of the National Aeronautics and Space Administration.

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## INTRODUCTION AND SUMMARY

Advanced focal plane concepts, incorporating two-dimensional arrays of VLWIR Ge:Ga or other extrinsic infrared detectors, are currently under study for cold-background astronomical applications such as SIRTf. This program of MOSFET characterization was undertaken to resolve certain critical electronic issues related to the feasibility of a promising design concept: "switch-sampled" operation.

Because of their extremely high impedance, low-background extrinsic devices have hitherto been used with contiguous, cryogenically operated, load resistors and MOSFET source-follower preamplifiers to minimize noise and maximize bandwidth. Under the extremely low operating temperatures required for state-of-the-art Ge:Ga operation (2.5 to 3.5 K), the MOSFET characteristics have been found to be subject to drifts. These drifts can cause sensor calibrations to be rather unreliable. Furthermore, as the number of detectors required in the arrays grows ever larger, the power dissipation of a system with a dedicated continuous operating preamplifier channel for each detector must eventually become untenable.

Operation in the switch-sampling mode may provide a solution to both problems. Here, the MOSFETs associated with a group of detectors share a common output source bus, and are "enabled" one at a time in an ordered sequence during the course of a data "frame". The load resistors of the conventional amplifiers are replaced by MOS switches. These are normally held in a nonconducting state so that the photocurrent in each detector is integrated at the input capacitance of its associated MOSFET. To "read" the signal on a given detector, its amplifier is enabled and the outputs are compared before and after the switch is momentarily turned on to reset the integration node to a constant reference voltage. The difference represents the integration of the photocurrent accumulated since the previous sampling of that detector.

In principle, this differential or correlated-double-sampling (CDS) process can be accomplished in a matter of microseconds. Many detectors can thus be multiplexed onto a single output channel with overall data rates of a

few tens of thousands of samples per second. As an example, if the whole readout cycle is accomplished in 60 microseconds ( $\mu$ s) or less, a row of 32 detectors could be operated at 500 frames per second with only slightly greater power dissipation than a single conventional detector channel with an inferior information bandwidth (BW). In addition, because the information is not contained in the absolute preamplifier output, but rather in the step effected in a matter of microseconds, the preamplifiers may be ac-coupled to the external CDS circuitry and the system is highly immune to normal drifts.

The scheme has been demonstrated in prototype form for shorter-wavelength extrinsic-silicon devices operating at somewhat higher temperatures. Critical to the feasibility of the scheme for the VLWIR applications that are contemplated are the ability to turn the MOSFETs (amplifiers, enable switches, and reset switches) on and off in reasonable time frames at the low operating temperatures desired, and the realization of noise levels of the same order as those achieved for continuously operating devices. The sequence of tests reported here was undertaken with the express purpose of resolving these issues.

Measurements were performed on three representative and applicable types of MOSFET devices available in chip form:

- a. The 3N163--a low-noise, low-capacitance, p-channel, enhancement-mode amplifier chip
- b. The 3N169--a low-power, moderately low-noise, n-channel, enhancement-mode amplifier or switch
- c. The M104--a very low-capacitance, p-channel, enhancement-mode switch.

These three types of devices have been used successfully for other cryogenic systems and may therefore be considered as prime candidates for the VLWIR focal plane application.

The relevant operating characteristics of the MOSFETs tested were found to be fully adequate at 2.8 to 3 K, the nominal temperature at which most of the measurements were made. Switching times were shown to be of the order of a few microseconds and, limited by the external-signal-processing bandwidth,

readout intervals as short as 50  $\mu$ s were easily demonstrated. Direct measurements at 2.8 K demonstrated that, with correlated double sampling, system noise should be limited by the cryoFET to values no greater than a few hundred electrons per sample, and that values as low as 100 electrons per sample should be achievable with selected devices. These values were independent of sample (frame) rate in the measured range from 10 to 1000 frames per second.

In short, a high-performance, low-power-dissipation, VLWIR mosaic using the switch-sampled readout architecture appears to be feasible from the purely electronic viewpoint, although certain other thermomechanical and packaging issues beyond the scope of this investigation may remain to be resolved.

## 2 STEADY-STATE CHARACTERISTICS

The current-voltage characteristics and output-noise spectra of several samples of the three device types selected were examined under steady-state operating conditions in order to provide a basis for comparison with low-duty-cycle performance data.

The chips were mounted with conductive epoxy on 0.015-in.-thick alumina-ceramic die carriers. These, in turn, were bonded directly to the copper test block, which was screwed to the Dewar cold finger. A calibrated temperature sensor (Allen Bradley carbon resistor) was mounted in the test block. The 0.0007-in.-diameter gold leads from the device were bonded to Ti/Au termination pads on the die carriers. The 0.001-in.-diameter gold leads from the die carriers, to either the external Dewar connections or other devices, were heat-sunk to the copper block. There was no way within the scope of this effort to determine the actual channel temperature when the devices were in operation, or even to ascertain the temperature of the substrate die. It is nevertheless reasonable to believe that the chips were as well heat-sunk as possible, and that the measurements are representative of the performance which might be expected from devices installed in a focal plane operating at the same nominal temperature.

## 2.1 3N163 Device

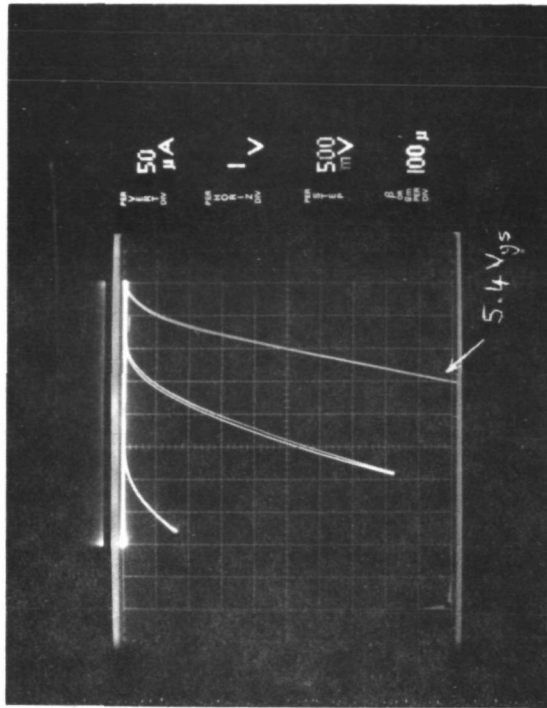
The 3N163 device is an unprotected, p-channel, enhancement-mode MOSFET characterized by a high transconductance ( $g_m$ ), with low input capacitance ( $C_{gs}$ ) and noise at cryogenic temperatures. It has been used extensively as a cryogenic preamplifier with extrinsic-silicon infrared detectors. When operated as a source follower (with the substrate and source connected), its input capacitance is typically in the range from 0.8 to 1.0 pF.

The I-V curves for a representative 3N163 chip (one of three tested) are shown in Figure 1. Little change was evident as the cryostage temperature was reduced from 5.0 K (the temperature achieved with the liquid-helium Dewar vessel atmospheric pressure) to 2.8 K (the minimum realized when pumping over the cryogen)\*. These I-V curves represent an extreme example of the anomalous  $V_{ds}$  threshold effect that is frequently observed in low-temperature operation and may be associated with carrier freezeout in the source (S) and drain (D) diffusions. The effect makes the 3N163 device inherently unsuited for use as a switch, but in no way limits its utility as an amplifier. Typically, the 3N163 is operated at a drain current between 100 and 200 microamperes and at a drain-to-source voltage ( $V_{ds}$ ) of about 5 volts. Power dissipation is thus usually between 0.5 and 1 mW per channel. Under this operating condition,  $g_m$  is of the order of 700 to 1000  $\mu$ mhos, and near-unity follower gain is achieved with a 10-kilohm or greater source impedance. A 25-kilohm source load was used in this measurement program.

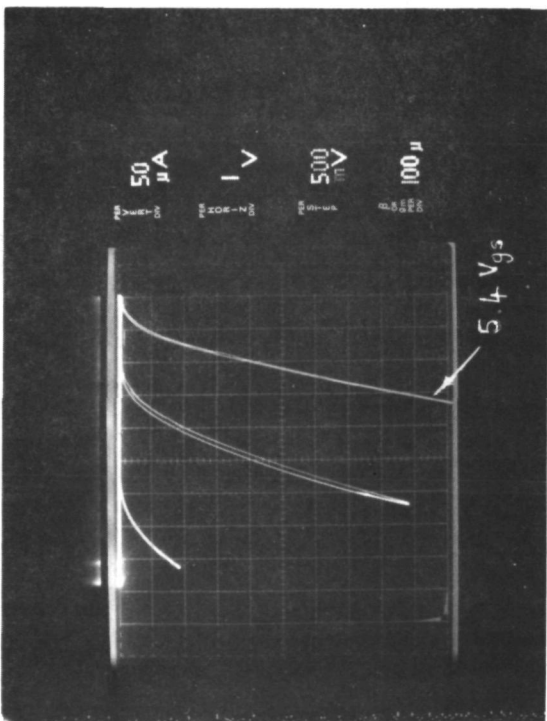
The noise spectra were measured in the range from 10 Hz to 100 kHz using the configuration shown in Figure 2. A Si:Bi detector element was provided to simulate a Ge:Ga detector and was zero-biased to eliminate thermal and background generation-recombination noise sources. The M104 switch (SW) was provided to simulate the reset switch of the switch-sampling readout configuration. The system calibration was checked by measuring the Johnson noise of a high-quality 1-megohm metal-film resistor.

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\* The nominal temperature of the pumped-over helium, as determined from pressure measurements, was 2.2 K.



- a. 5.0 K  
10 steps x 0.5 V  
0.4 V dc



- b. 2.8 K  
10 steps x 0.5 V  
0.4 V dc

Figure 1 Current-Voltage Characteristics for 3N163 CryoFET

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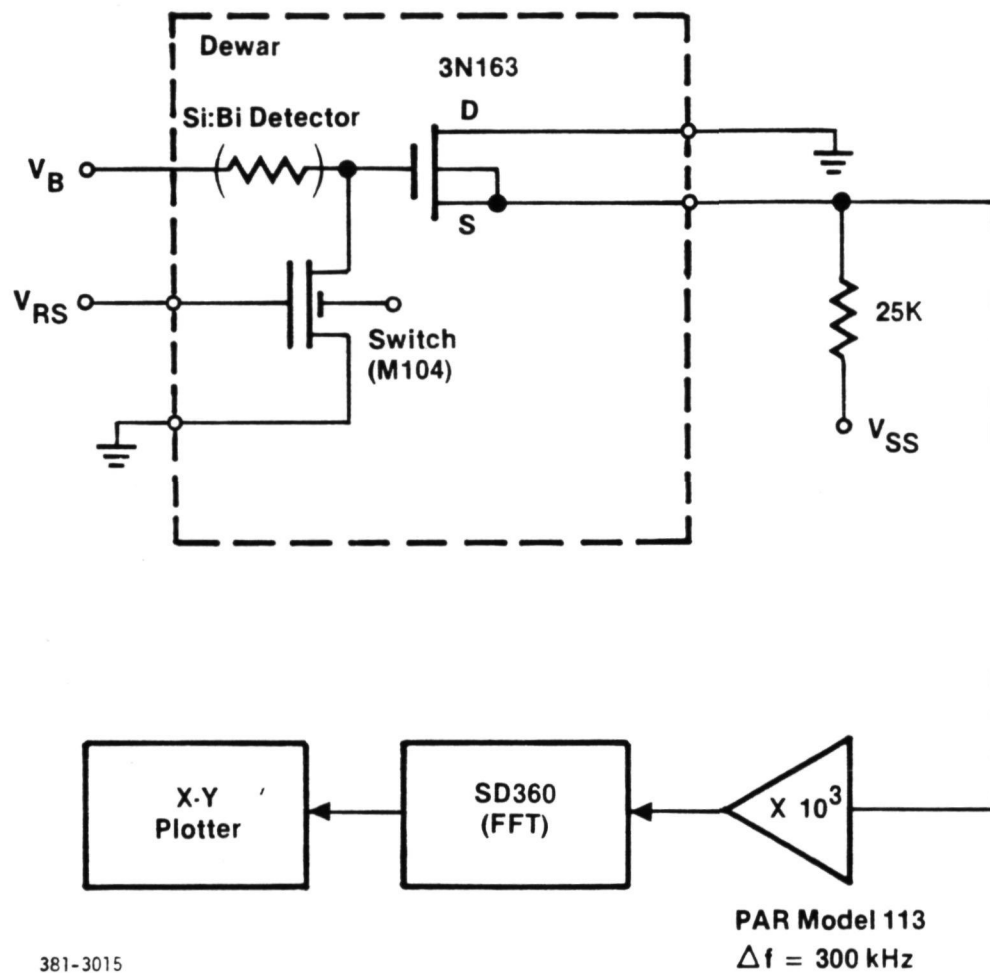


Figure 2 Noise-Measurement Setup for 3N163 Devices



The noise spectra shown in Figure 3\* are believed to be representative of the range of values achievable for the 3N163 device. Chip 3 is probably typical of the present state of the art. Noise levels of this order, however, can be achieved only by selecting the best 10% of devices from a lot. Devices 1 and 2 represent the "typical" range realizable in up to 80% of a lot. None of the chips was particularly temperature-dependent, a 10 to 20% degradation in noise being experienced upon cooling from 5 K to 2.8 K (marked 3 K on the charts).

The noise of all three chips was slightly dependent on the impedance at the gate, as is usually the case at higher temperatures also. With the M104 switch nonconducting, the impedance to ground at the gate is determined by the sum of the switch, detector, and MOSFET input capacitances. These values were approximately 0.25, 0.4, and 0.8 pF, respectively, for a total of about 1.5 pF for the 3N163. When the switch was conducting and the effective gate-to-ground impedance was reduced to the order of a few kilohms, a noise reduction of approximately 20% was manifest for Chip 1. This is typical of Aerojet's previous experience at higher temperatures. The difference may be considered as being due to a small equivalent gate-leakage-noise current.

## 2.2 3N169 Device

The 3N169 is an n-channel enhancement-mode device. Like the 3N163, it has sufficient transconductance so that it can be used as an amplifier at cryogenic temperatures. Although neither the noise nor the capacitance of typical 3N169 chips is as low as that of the p-channel devices\*\*, the n-channel MOSFET has the advantage of a significantly lower threshold voltage and more-conventional I-V characteristics. It can be operated without severe degradation, at a dissipation an order of magnitude lower--say 50 to 100  $\mu$ A and 1 to 2 volts ( $V_{ds}$ ).

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\* These and other noise spectra reproduced here have been "cleaned up" by deleting from the random-noise spectra the peaks due to the 60-Hz line harmonics (and other coherent interference sources).

\*\*Aerojet has measured one lot of 3N169 devices that achieved near parity with the 3N163, but no other chips of this quality have been found since.

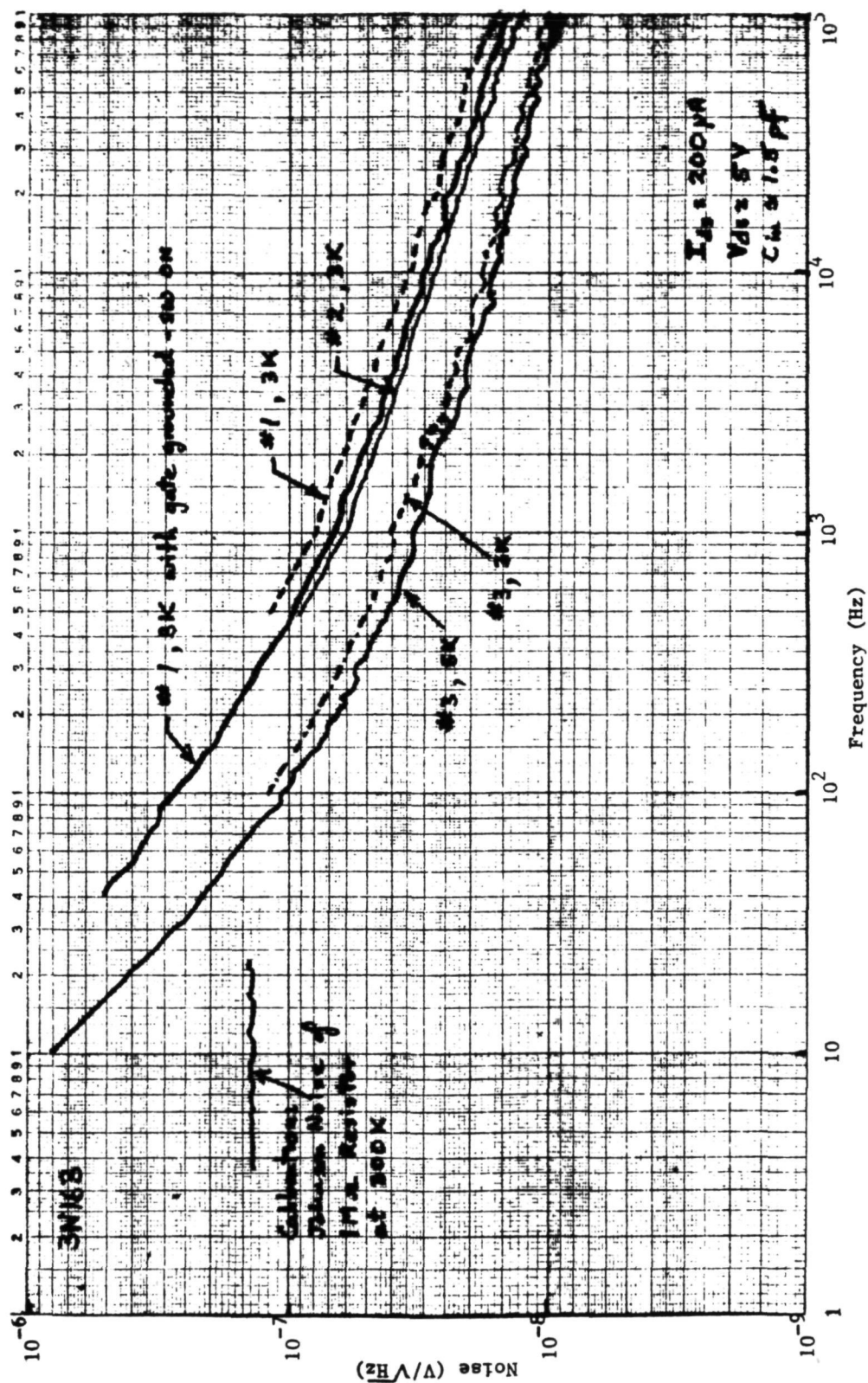


Figure 3 Noise Spectra for Three 3N163 Chips

The I-V characteristics shown in Figure 4 are apparently almost independent of substrate temperature in the 5- to 2.8-K range. The characteristic is also very similar to that reported by Lepselter and Sze\* for Schottky-contact FETs; this suggests that carrier freezeout in the source and drain diffusions may also be occurring in this device, although the effect is not as pronounced as for the 3N163.

Noise spectra for the n-channel amplifier at 2.8 K and at various different drain-current operating points are presented in Figure 5. The measurement setup shown in Figure 2 was also used in this case. Unfortunately, the devices tested were not particularly good ones. The 3N169 noise is generally a factor of 2 or so better than that shown here. Degradation from 5 to 3K was no more than 15%.

The input capacitance of the 3N169 is about 2 pF, giving a total input capacitance in excess of 2.5 pF when combined with a detector and switch. The equivalent input-noise current ( $\propto \epsilon_n \cdot C_{in}$ ) of the 3N169 is thus more than an order of magnitude higher than that of the 3N163.

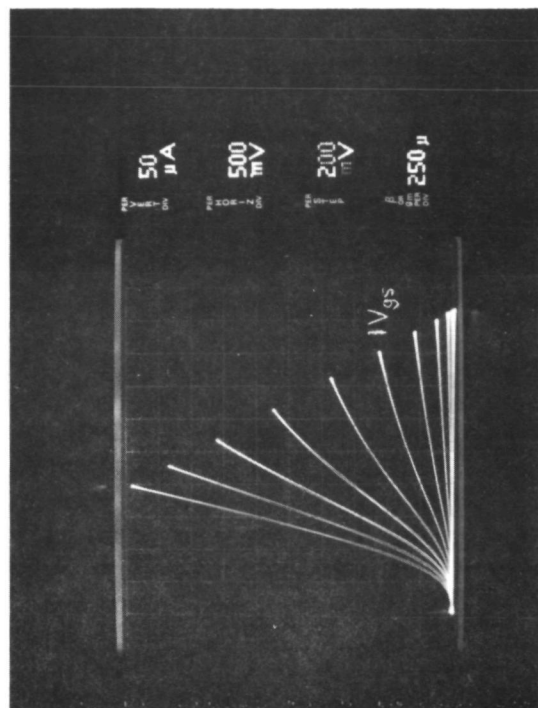
### 2.3 M104 Device

The M104 was selected for use as a cryogenic switch with extremely low drain-to-source shunt capacitance (0.6 pF) when operated with the substrate floating. Current-voltage characteristics for two M104 chips at 3 K are shown in Figure 6. Of the three device types tested, the M104 exhibits the greatest similarity to the classical I-V characteristics expected at 300 K. Although selected for use as a cryogenic switch, its transconductance of 300 to 400  $\mu\text{mhos}$  qualifies it for use as an amplifier if necessary.

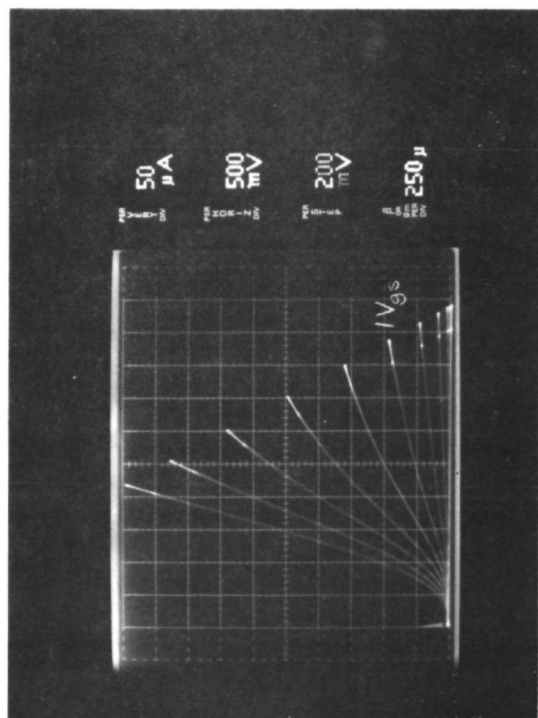
Noise spectra for an M104 are shown in Figure 7. In contrast to the other devices tested, the noise of the M104 apparently decreased with decreasing temperature from 5 to 2.8 K. Although this result was confirmed by repeated measurement on several chips, a corresponding decrease was not observed for the

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\* M. P. Lepselter and S. M. Sze, Proc. IEEE, Vol. 56 (August 1968).



- a. 5.0 K  
10 steps x 0.2 V  
0 V dc



- b. 2.8 K  
10 steps x 0.2 V  
0 V dc

Figure 4 Current-Voltage Characteristics of 3N169 CryoFET

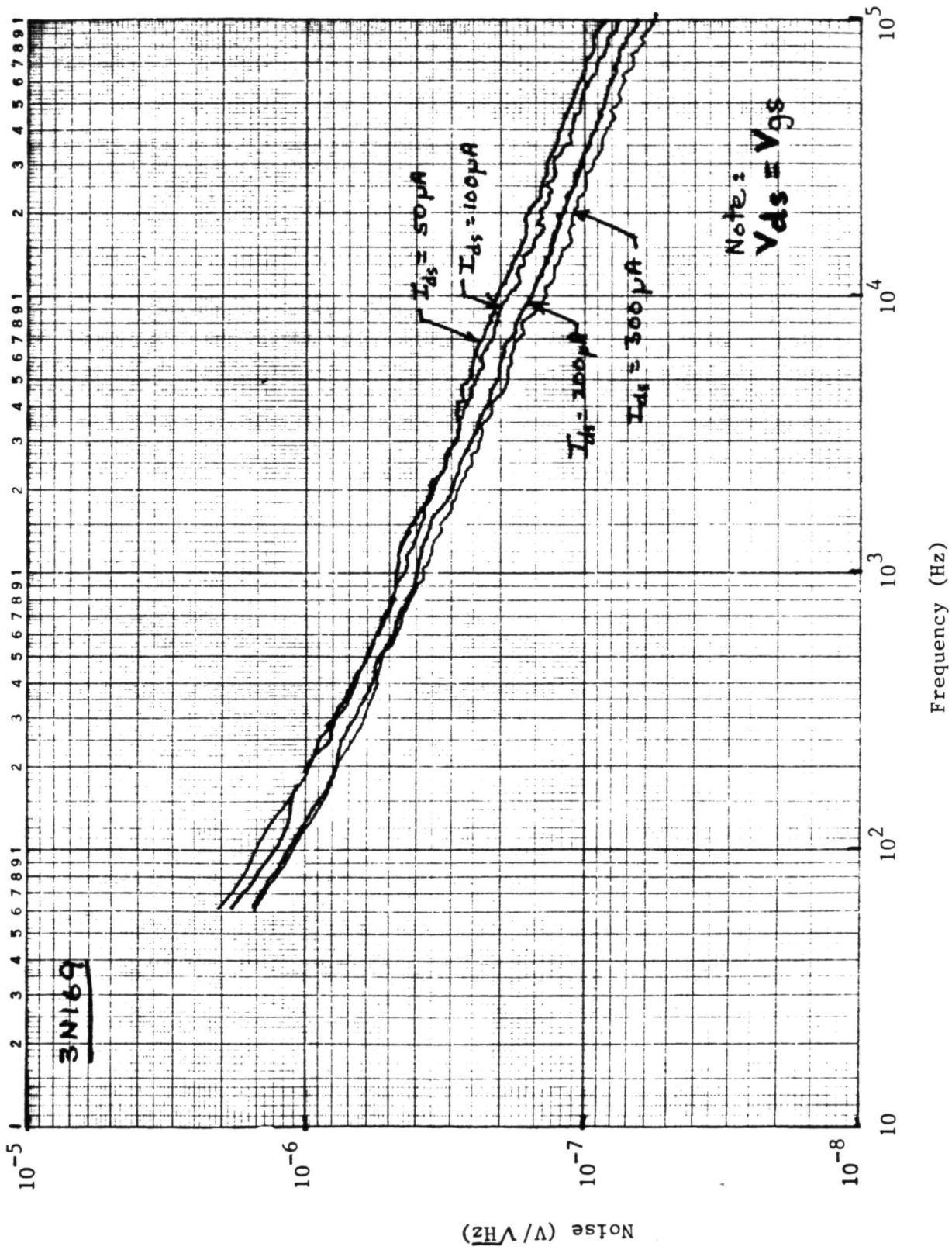
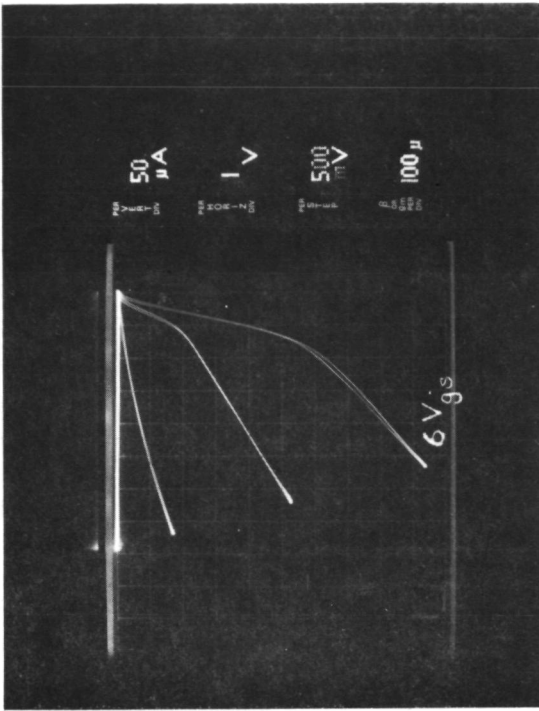
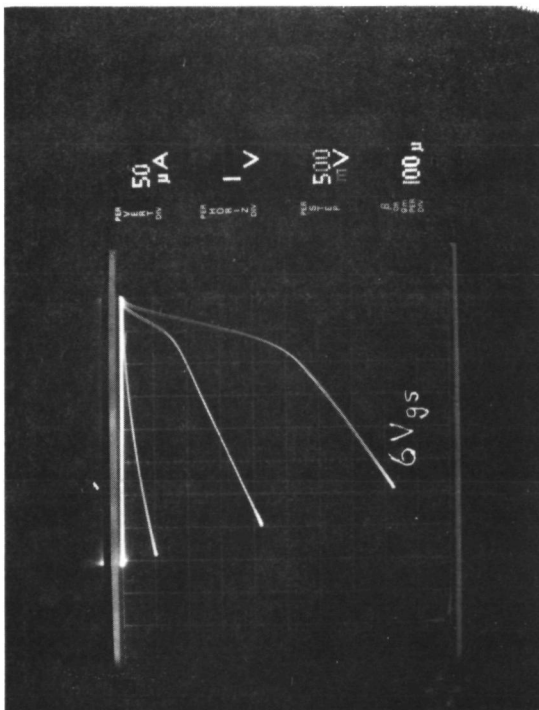


Figure 5 Noise Spectra for 3N169 (Chip 2) at 2.8 K



a. Chip 1  
10 steps x 0.5 V  
1.0 V dc



b. Chip 2  
10 steps x 0.5 V  
1.0 V dc

Figure 6 Current-Voltage Characteristics of M104 Chips at 3 K



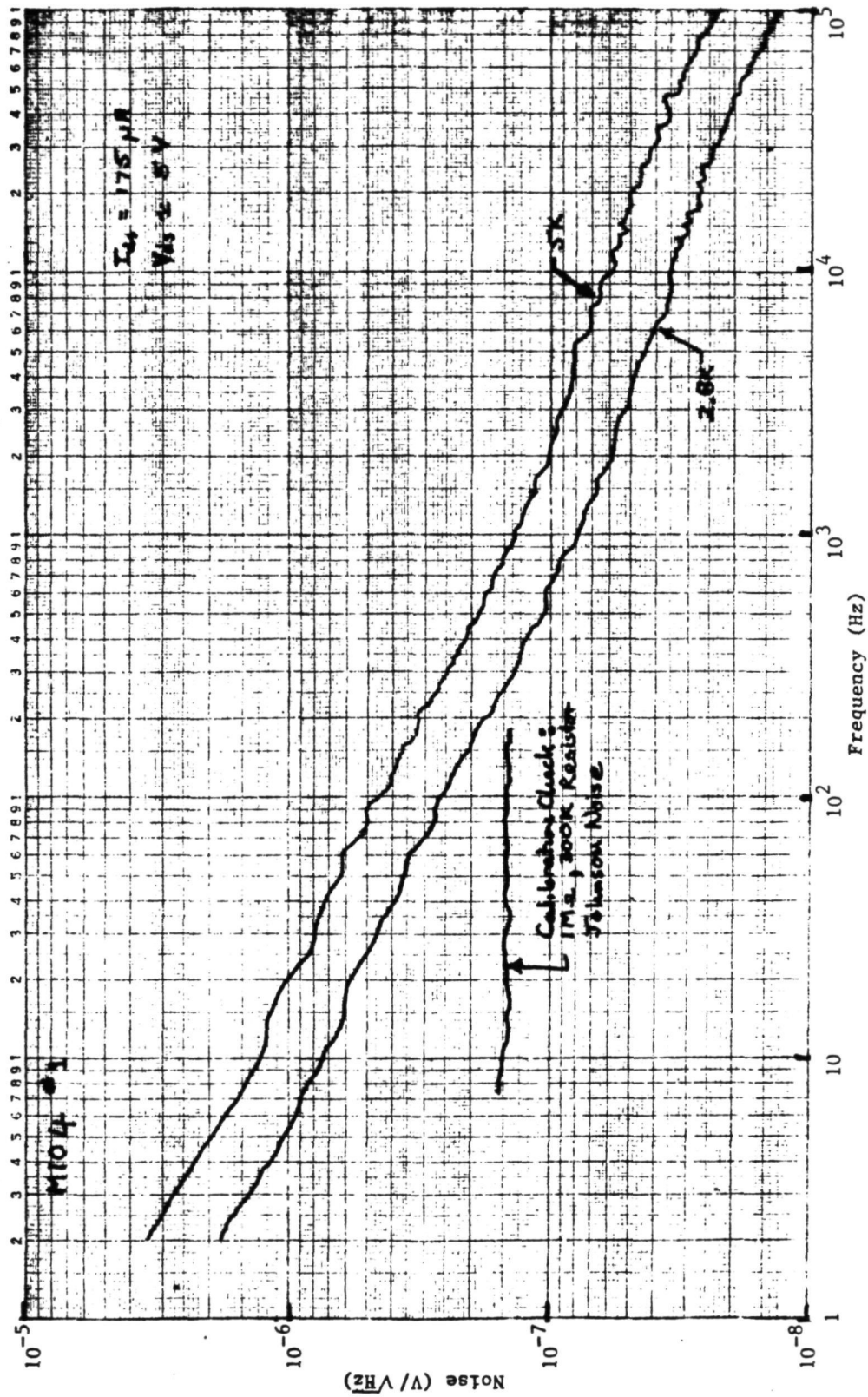


Figure 7 Noise Spectra for M104 Switching MOSFET

differentially sampled (CDS) data for this device (e.g., see Section 3). Resolution of this apparent discrepancy was not possible within the scope of this effort. It is not likely, however, that the conclusions drawn would be profoundly affected in any event.

### 3 CORRELATED DOUBLE SAMPLING

Correlated double sampling or delayed differential sampling was performed on the outputs of the MOSFET, while continuously running, in order to provide a direct comparison with theoretical predictions based on the noise spectra reported above. The action of the CDS circuit on a time waveform  $n(t)$  produces samples of the new waveform:

$$n_1(t) = n(t) - n(t-\Delta) \quad (1)$$

where  $\Delta$  is the correlation or delay interval. Because this new waveform,  $n_1(t)$ , represents the net change in  $n(t)$  over the preceding interval ( $\Delta$ ), components of  $n(t)$  at frequencies small compared with  $1/2\Delta$  tend to be suppressed.

More generally, the action of any signal-processing circuit on an input waveform  $n(t)$  may be defined in the time domain in terms of the convolution:

$$n_1(t) = \int_0^{\infty} n(t-T) f(T) dT \quad (2)$$

where  $f(T)$ , the weighting or filter function of the signal processing, is defined within the interval  $0 \leq T \leq \infty$ . In the case of a single-pole analog filter with gain  $A$  and response time  $\tau_0$ , for example, the function  $f(T)$  would be of the form

$$f_1(T) = \frac{A}{T_0} \exp(-T/\tau_0) \quad (3)$$

For the CDS process,  $f(T)$  can be defined in terms of the delta functions at  $T = 0$  and  $T = \Delta$  in the form

$$f_2(T) = \delta(T) - \delta(T-\Delta) \quad (4)$$

The power spectrum of the convolution may be written in terms of the product of the transforms of the convolved functions. Thus, in the frequency domain, the spectrum of the differentially sampled waveform  $n_1(t)$  (for continuous sampling) would be

$$N_1(\omega) = N(\omega) F(\omega) \quad (5)$$

where  $F(\omega)$ , the Fourier transform of the weighting function  $f(T)$ , may be viewed as the transfer function of the processing circuit. In the CDS case, it is easily derived as

$$F_2(\omega) = \sqrt{2} \sin(\omega\Delta/2) \quad (6)$$

Similarly, of course, the transfer function of the single-pole circuit is

$$F_1(\omega) = A (1 + \omega^2 \tau_o^2)^{-1/2} \quad (7)$$

At the output of an idealized, continuously operating, CDS system with a delay interval of  $\Delta$ , and preceded by a single-pole amplifier with a bandwidth (BW) of  $f_o$  and a gain of  $A$ , the input-noise spectrum  $N(f)$  of the waveform  $n(t)$  should be transformed to a new spectrum of the following form:

$$N_1(f) = N(f) \sqrt{2} A (1 + f^2/f_o^2)^{-1/2} \sin(\pi f \Delta) \quad (8)$$

The rms (1 $\sigma$ ) broadband amplitude,  $\bar{N}_1$ , of the waveform having this spectrum is, as usual, given by

$$\bar{N}_1^2 = \int_0^\infty N_1^2(f) df \quad (9)$$

In a real system, of course,  $n_1(t)$  would not be continuously developed as an analog waveform, but rather samples would be generated at discrete times,  $t_n$ , at intervals determined by the sampling rate,  $f_s$ . The rms-amplitude variation of the sequence of samples should, however, be the same as that for the idealized continuous waveform.

To perform the CDS measurements, Aerojet used a circuit under development for operating accumulation-mode charge-injection-device (AMCID)

mosaics. Its essential operational features are illustrated in Figure 8. The output of the MOSFET under test [shown as a 3N163 device with a detector and reset (RS) switch at the gate] is ac-coupled at about 1 kHz into a gain-of-200 amplifier. The correlated double sample is generated by referencing the amplifier output to ground by momentarily turning on the switch (S1) and then, after the required delay ( $\Delta$ ), activating the sample and hold [S/H (S2)]. This sample amplitude is held at the system output until it is updated  $f_s^{-1}$  seconds later. The output waveform from the system is therefore a random "square" wave of frequency  $f_s$  whose rms amplitude is presumably identical to that of the idealized CDS noise waveform,  $n_1(t)$ , discussed above.

The spectrum of such a waveform should be of the form

$$S(f) = N_o \frac{\sin(\pi f/f_s)}{\pi f/f_s} \quad (10)$$

with minima such that  $S(f) = 0$  at  $f = f_s, 2 f_s, \text{etc.}$

The rms variation of the samples may be deduced from the measured spectra by using the following relationships:

$$\bar{N}_1^2 = \int_0^\infty S^2(f) df = N_o^2 f_s / 2 \quad (11)$$

Equations 8, 9, and 11 provide the basis for comparing CDS measurements with the original MOSFET noise spectra.

The quantity  $\bar{N}_1$  represents the limiting noise for measurement of the voltage step generated when the photocurrent sample accumulated at the MOSFET gate is discharged to ground by the reset switch. It is therefore useful to relate  $\bar{N}_1$  to an equivalent rms-noise charge ( $\bar{Q}$ ), or number of electrons ( $\bar{N}_e$ ) at the MOSFET gate. The relationship is of the following form:

$$\bar{Q} = 1.6 \times 10^{-19} \bar{N}_e = \frac{\bar{N}_1 C_{in}}{A_o} \quad \text{coulombs/sample} \quad (12)$$

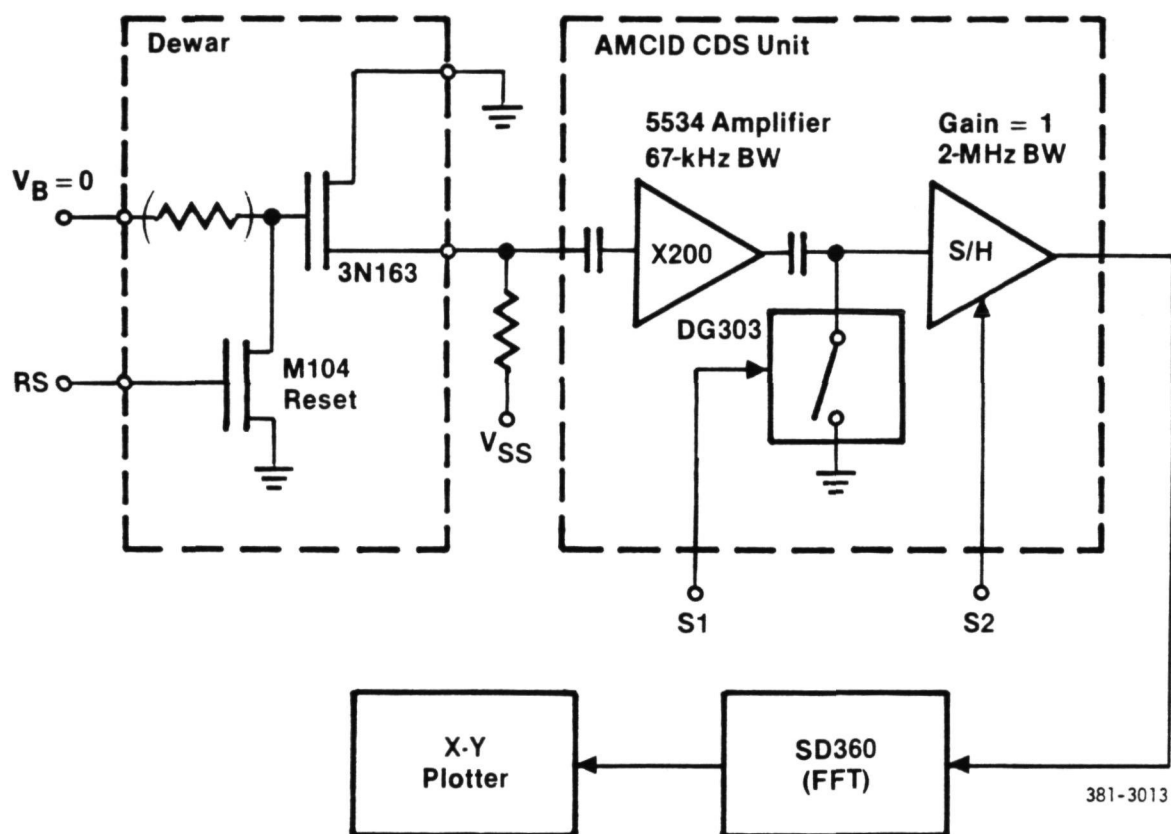


Figure 8 CDS Measurement System

where  $C_{in}$  is the MOSFET input capacitance and  $A_o$  is the overall amplifier gain, including that of the source follower itself (which will be slightly less than unity).

Measured CDS noise spectra for a 1-kHz sampling rate and a 10- $\mu$ s correlation interval ( $\Delta$ ) are shown in Figure 9 for all three MOSFET types. They are of the expected  $(\sin x)/x$  form and no significant change was observed as the temperature was reduced from 5 K to 2.8 K. For  $\Delta$  equal to 10  $\mu$ s, the CDS transfer function is expected to peak at 50 kHz ( $1/2\Delta$ ) and to be down by  $\sqrt{2}$  at 25 kHz. On the high-frequency side, the gain amplifier effectively limits the bandwidth of the system at 67 kHz. The effective bandwidth represented by Equation 8 is therefore approximately 40 kHz, peaking at about 50 kHz. Because the MOSFET noise spectra (i.e., Figures 3, 5, and 7) are not strongly frequency-dependent in this range, Equation 9 may be crudely estimated in the form

$$\overline{N}_1^2 \approx 2A^2 (4 \times 10^4) N^2(50K) \quad (13)$$

where  $N(50K)$  is the MOSFET-noise spectral density at 50 kHz, the nominal peak of the Equation 8 spectrum.

For the gain-of-200 system, we therefore expect

$$\overline{N}_1 \approx 5.6 \times 10^4 N(50K) \quad (14)$$

In turn, we may relate the amplitude ( $N_o$ ) of the measured CDS noise spectrum to the MOSFET noise using Equation 11. For a 1-kHz sample rate, we expect

$$\overline{N}_1 = 22.4 N_o \approx 5.6 \times 10^4 N(50K)$$

so that, from Equation 11,

$$N_o \sim 2.4 \times 10^3 N(50K) \quad (15)$$

The measured values of  $N_o$  and  $N(50K)$ , together with estimates of the corresponding noise-equivalent charge at the input to the MOSFET, are presented in Table 1.



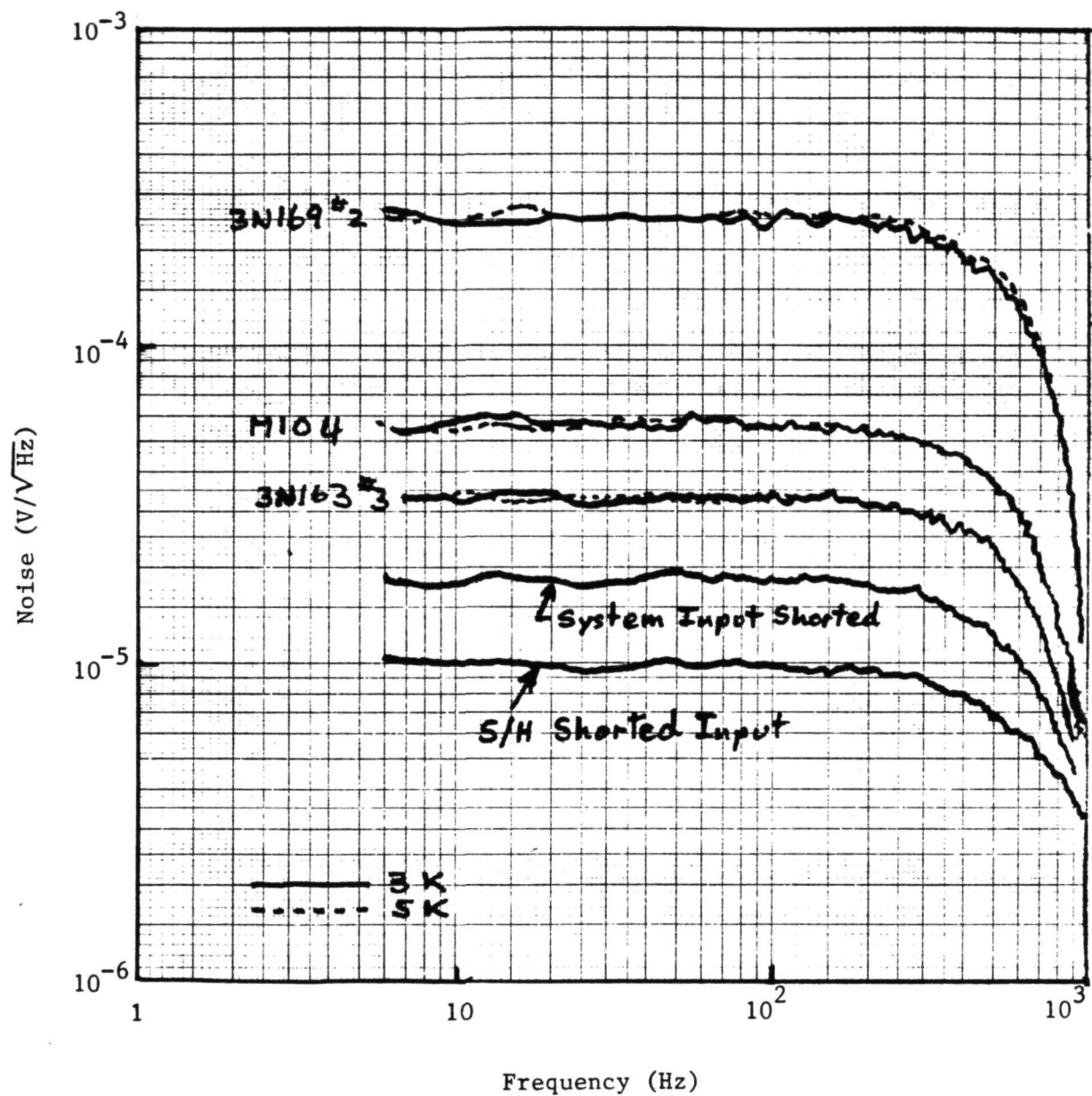


Figure 9 Spectra of Correlated-Double-Sampled FET Noise Waveforms

Table 1 CDS Noise Levels for Continuously  
Running FETs at 3 K

Parameter	3N163 Chip 3	3N169 Chip 2	M104 Chip 1
FET noise $[N(50K), V/\sqrt{Hz}]$	$1.2 \times 10^{-8}$	$1.0 \times 10^{-7}$	$1.9 \times 10^{-8}$
CDS noise $(N_o), V/\sqrt{Hz}$	$3.4 \times 10^{-5}$	$2.5 \times 10^{-4}$	$5.6 \times 10^{-5}$
$N_o/N(50K)$	$2.9 \times 10^3$	$2.5 \times 10^3$	$2.9 \times 10^3$
$C_{in}, pF^*$	1.5	2.5	1.5
FET gain	0.94	0.85	0.9
$I_{ds}, \mu A$	200	100	175
Equivalent rms input noise:			
$\bar{Q}$ , coulombs/sample	$6 \times 10^{-18}$	$8 \times 10^{-17}$	$1.0 \times 10^{-17}$
$\bar{N}_e$ , electrons/sample	37	500	63
* Input capacitance of FET with detector and M104 reset switch.			

The agreement between the predicted value ( $2.4 \times 10^3$ ) and the measured value ( $2.5$  to  $2.9 \times 10^3$ ) of the ratio  $N_o/N(50K)$  is excellent in view of the crudity of the estimating procedure. The discrepancy implies a slightly wider effective noise bandwidth (Equation 8) than the 25- to 67-kHz nominal values assumed, and/or a higher peak in-band FET-noise amplitude. Because the MOSFET noise tends to increase toward lower frequencies, it is indeed to be expected that the approximations used will underestimate both parameters. Extension of the nominal low end of the bandpass from 25 kHz to 20 kHz, and assumption of a 40-kHz rather than a 50-kHz peak, is sufficient to resolve the discrepancy. That Equation 11 is indeed approximately correct, and that the CDS process does strongly attenuate the low-frequency  $1/f$  components of the input waveforms, is confirmed by the absence of any apparent low-frequency correlation (i.e.,  $1/f$  component) in the CDS output spectra.

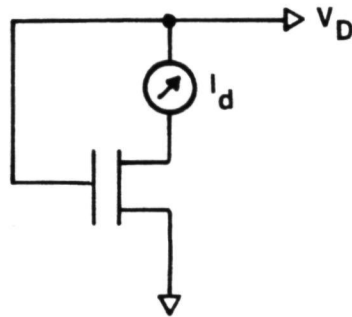
Conversion of the  $N_o$  values to broadband rms sample-noise indicates that, if there were no degradation due to the switching action, noise levels of less than 40 electrons per sample might be achievable with selected devices and that values of less than 100 electrons per sample could be realized with run-of-the-mill M104 chips.

#### 4 SWITCHING AND SWITCH SAMPLING

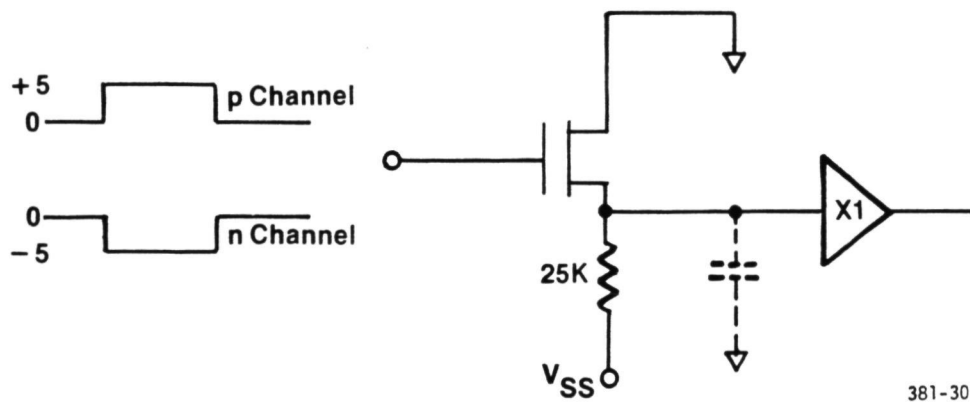
In order to multiplex several detector channels on a single output channel it will be necessary to switch the source-follower MOSFETs on and off so that the output bus may be time-shared. Two important basic questions arise in this connection:

- a. Can the FETs be turned on and off, and with sufficient speed, at the very low temperatures required?
- b. To what extent, if any, is the noise of the MOSFET degraded by so doing and, more to the point, to what extent are CDS output noise levels degraded?

To investigate basic switching characteristics at cryogenic temperatures, devices of each type were connected as shown in Figures 10a and 10b for static and dynamic testing, respectively. The static I-V characteristics of the switches, shown in Figure 11, illustrate clearly the lower threshold of the 3N169.



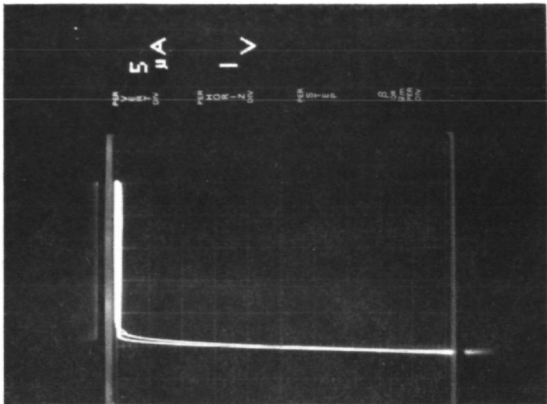
a. Static Characteristics



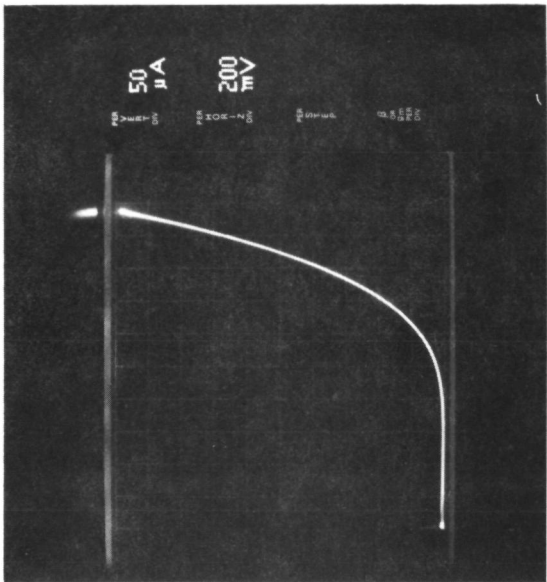
381-3012

b. Dynamic Characteristics

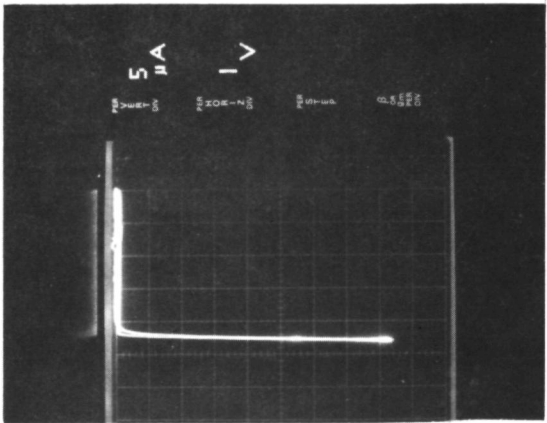
Figure 10 Measurement Setups



M104 No. 1



3N169 No. 2



3N163 No. 3

Figure 11 Static Switch I-V Characteristics at 2.8 K

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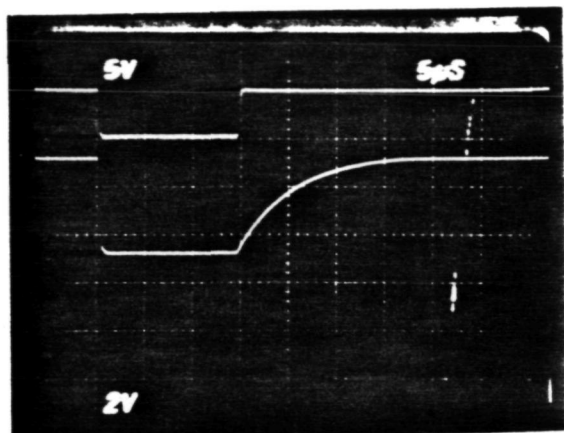
The turn-on and turn-off characteristics measured for each type of MOSFET are shown in Figure 12. The FETs were turned on with a 15- $\mu$ s square 5-volt pulse (positive or negative as appropriate) repeated at a 100-Hz rate. With a 10-ms "off" time between pulses, one may be reasonably sure that each device would be very close to the nominal 2.8-K substrate temperature when turned on. The turn-on time was 1  $\mu$ s or so for all three devices. Turn-off apparently required of the order of 10  $\mu$ s.

It is believed that both turn-on and turn-off were actually limited by charging of the output line capacitance, and do not represent the limit of performance at cryogenic temperatures. When the MOSFET is on, the output impedance is  $1/g_m$  (of the order of 1 to 3 kilohms), and when off, the circuit is ac-grounded through the 25-kilohm source resistor. The output line capacitance of about 300 pF would thus be expected to produce turn-on and turn-off time constants of the order of 0.5 and 7  $\mu$ s respectively, consistent with the observations.

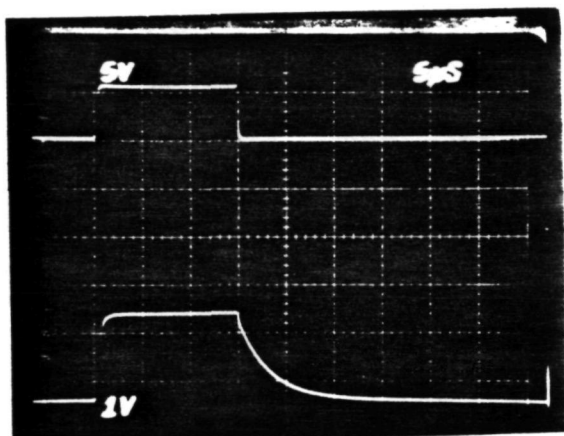
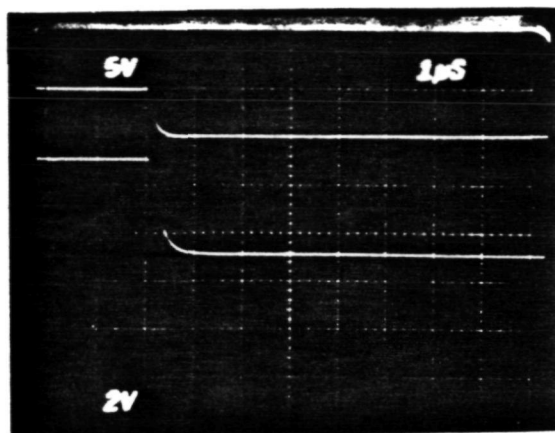
To investigate multiplex operation, two test FETs of the same type were connected with M104 enable and reset switches in the circuit shown in Figure 13. The subject of the tests was the chip designated as Amplifier 1. It could be operated continuously with the drain grounded, or could be "enabled" by applying +5 volts to the gate of the M104 switch (EN1). Through EN1 the chip could be switched on and off at will. To simulate time-shared operation, a low-duty-cycle square wave was applied to the gate of EN1, typically turning the amplifier on for 50  $\mu$ s and off for 950  $\mu$ s. This particular 5%-duty-cycle operation simulates the multiplexing of 20 detectors at a 1-khz frame rate.

In order to maintain the dc level of the output, and to prevent saturation of the ac-coupled amplifier, the other 19 "detectors" were represented by Amplifier 2, whose enabling switch (EN2) was driven with a waveform complementary to that driving EN1--i.e., on for 950  $\mu$ s and off for 50  $\mu$ s. For convenience, the gate of this second amplifier chip was dc-biased to eliminate the offsets due to differences between the thresholds of the two amplifiers.

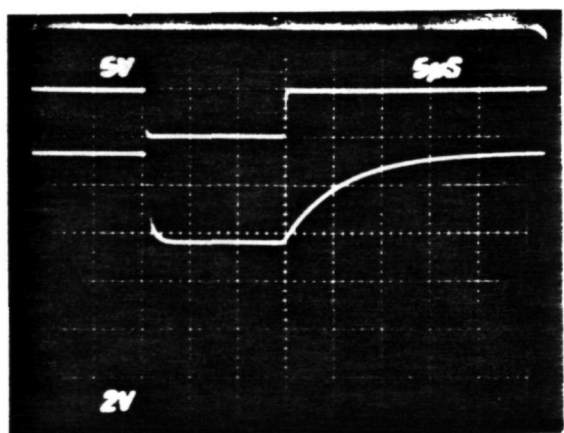
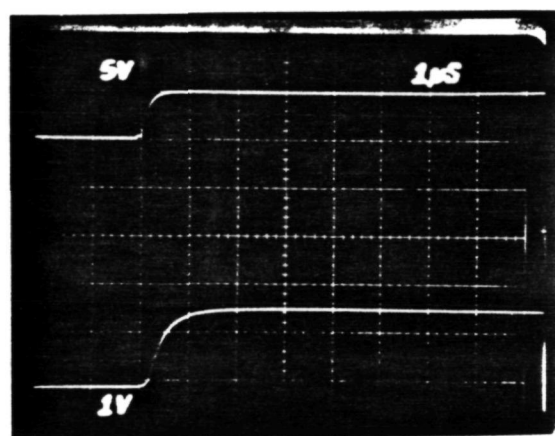




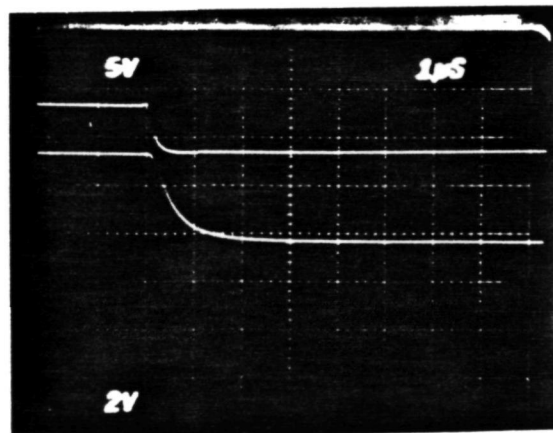
3N163 No. 3



3N169 No. 2

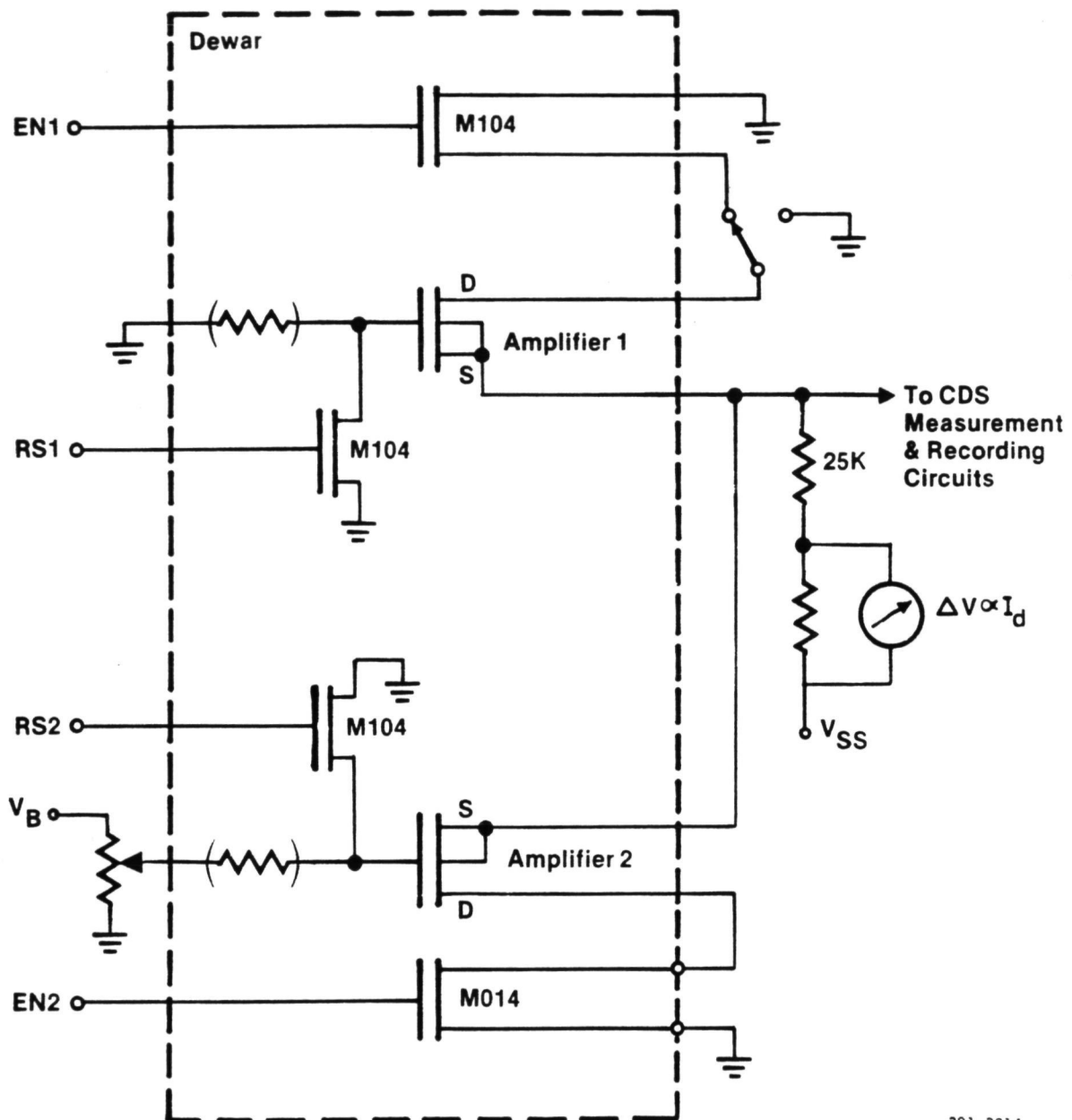


M104 No. 1



381-301a

Figure 12 Dynamic Switch Characteristics at 2.8 K



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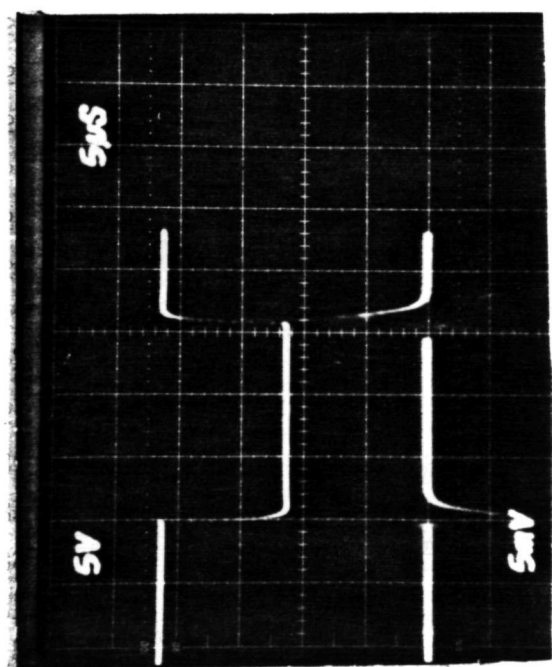
Figure 13 Multiplexer-Simulation Circuit

Representative waveforms recorded at the MOSFET source or sources and at the output of the (X200, 67-kHz-bandwidth) gain amplifier of the CDS measurement system are reproduced in Figure 14. In each photograph the lower trace records the system output and the upper trace reproduces the enable logic. As Figure 14a illustrates, the transients associated with MOSFET switching can be decayed sufficiently in 5  $\mu$ s for a 15- $\mu$ s enable period to be adequate for CDS sampling--i.e., up to 70,000 samples per second. However, an amplifier with a very wide bandwidth would be required, at the expense of overall CDS noise. Using the experimental CDS system with its 67-kHz amplifier bandwidth, the transients are extended to 10  $\mu$ s (e.g., Figures 14c, d). A total enable time of 50  $\mu$ s is demonstrably sufficient even for the rather slower n-channel amplifier (Figure 14b).

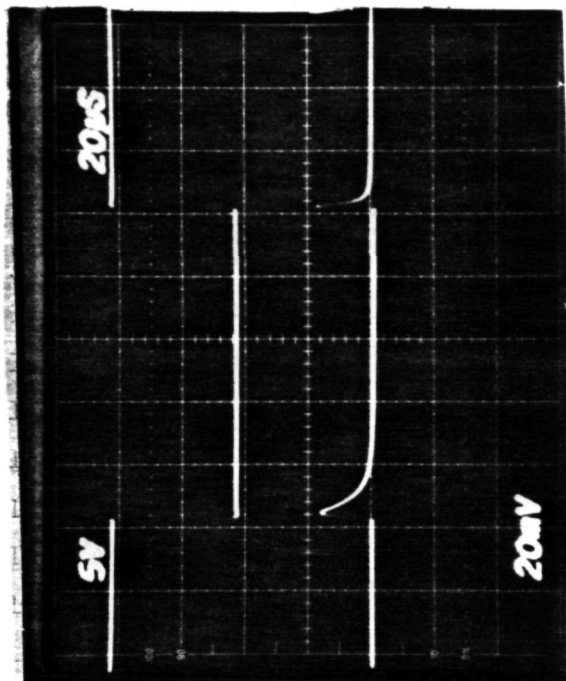
In this time-shared configuration, CDS noise measurements were made for three representative chips--3N163 No. 3, 3N163 No. 1, and 3N169 No. 2. Sampling was performed while the MOSFET was enabled in the low duty cycle described above, and continuous drain-grounded operation was also monitored for comparison. Data for the two 3N163 chips are shown in Figure 15. Although their noise amplitudes differ by about a factor of 2 when continuously running--consistent with the basic MOSFET-noise data of Figure 3--their low-duty-cycle CDS-noise spectra are almost identical. The output-noise level ( $\bar{N}$ ) is approximately  $1.9 \times 10^{-3}$  volt in both cases, corresponding to an equivalent input charge of  $1.5 \times 10^{-17}$  coulomb-- or slightly less than 100 electrons per sample.

For the 3N169, the CDS noise with low-duty-cycle operation was again only slightly greater (Figure 16) than for continuous operation. In this case, however, there is evidence of low-frequency sample-to-sample correlation. The output noise level here--about 7.2 rms mV per sample--corresponds to an input-sample noise of about  $10^{-16}$  coulomb or 600 electrons/sample.

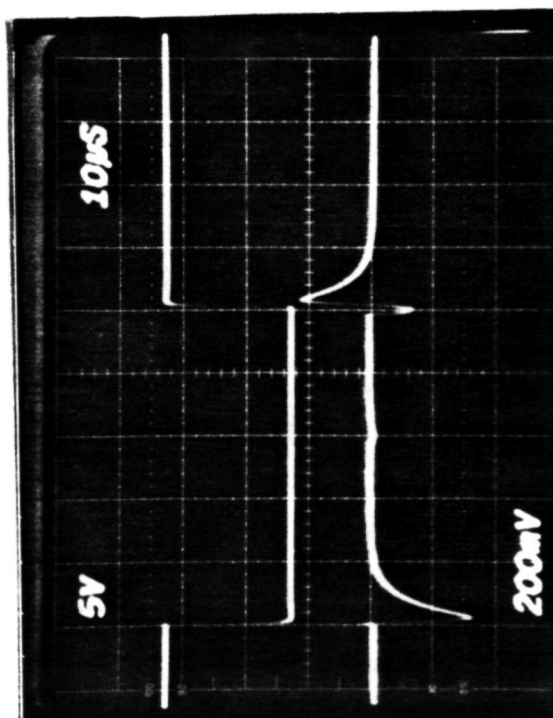
Additional data were acquired for the 3N163 No. 2 chip using varying sample rates, correlation intervals, and enable times. The wideband (sample) noise,  $N_o \sqrt{f_s}/2$ , was found to be independent of sample rate. This is to be expected because the power spectrum of the waveform resulting from idealized



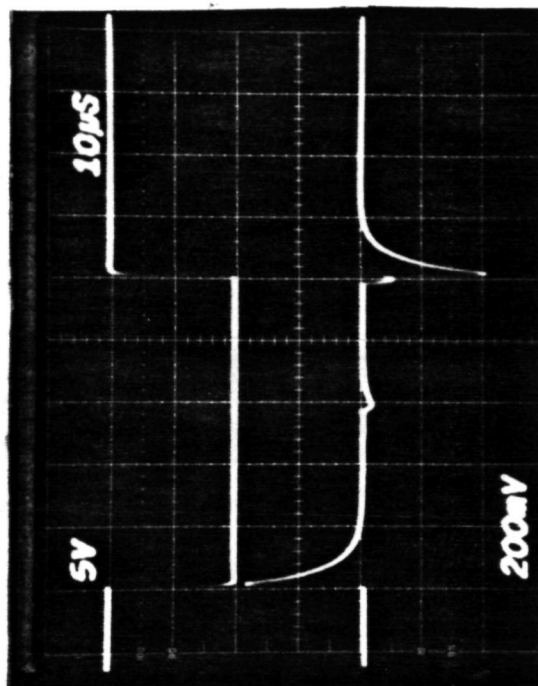
a. 3N163 No. 1--Source Output



b. 3N169 No. 2--Source Output



c. 3N163 No. 1--CDS Amplifier Output



d. 3N163 No. 3--CDS Amplifier Output

Figure 14 Time-Shared MOSFET Operation at 2.8 K

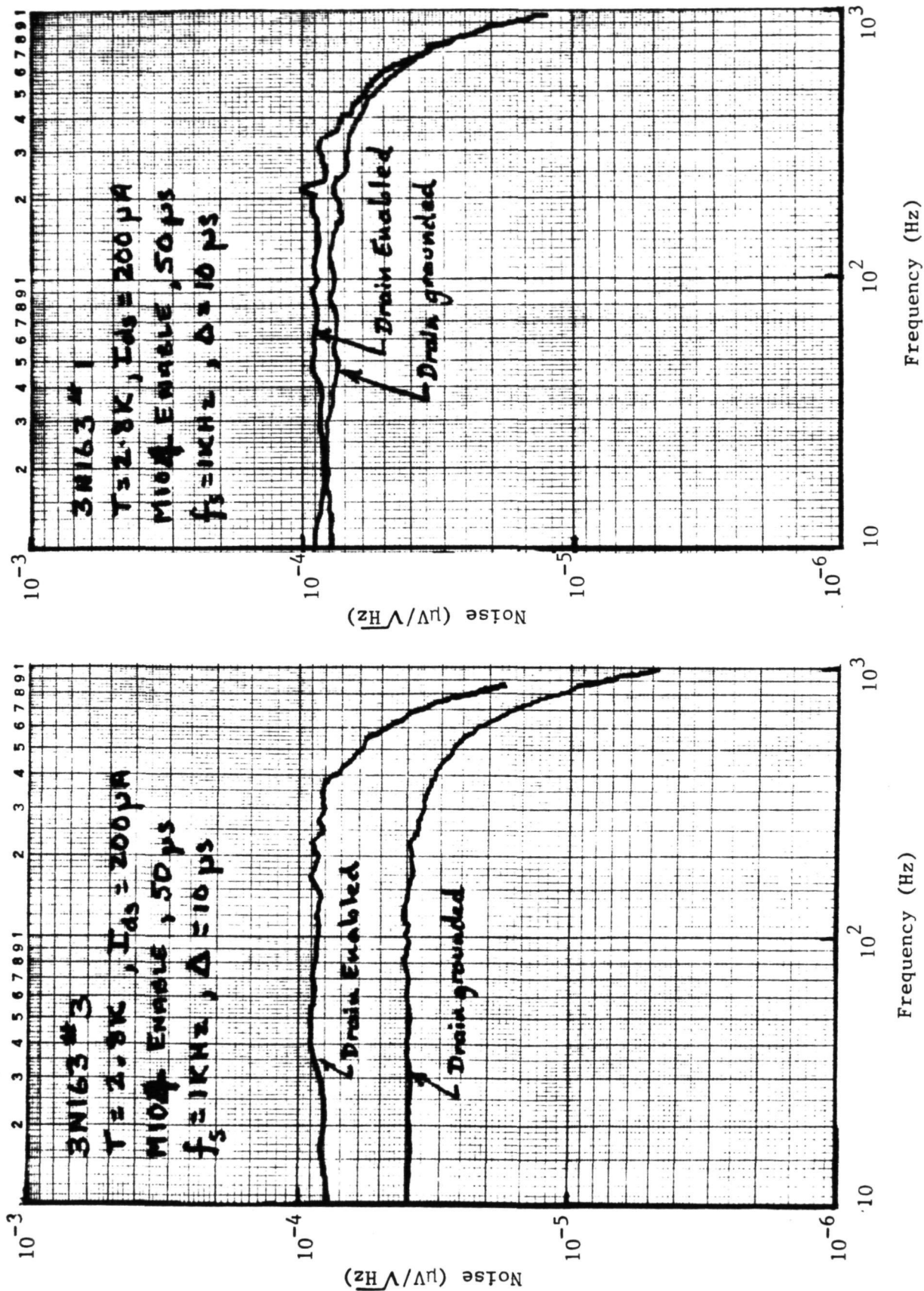


Figure 15 CDS Noise for Time-Shared Operation

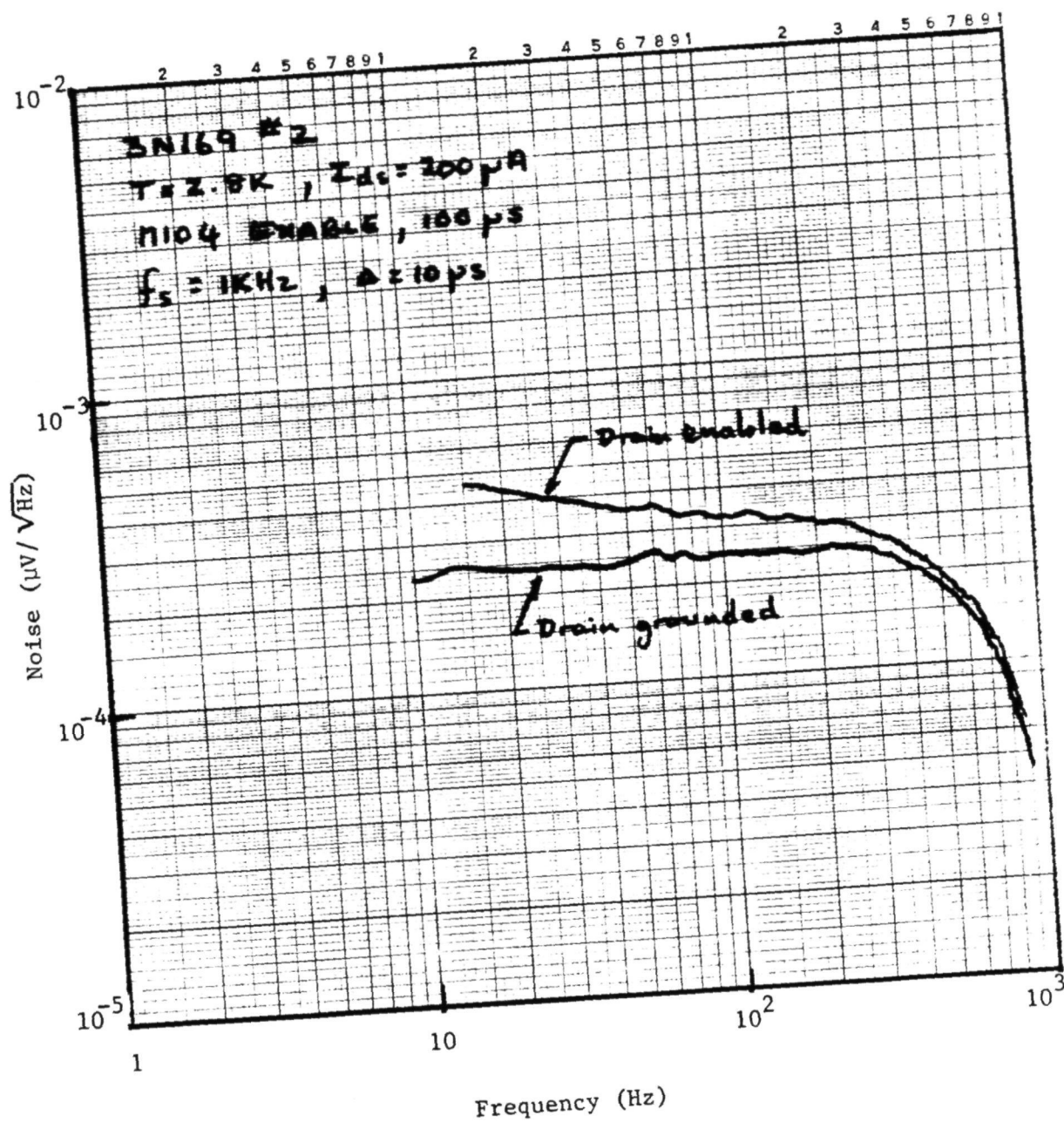


Figure 16 Time-Shared CDS Noise for 3N169 No. 2 at 2.8 K



CDS processing should be dominated by high frequencies. Consequently, no correlation should exist at the comparatively low sample intervals used, and the amplitude distribution of all sufficiently large sample ensembles should be identical--regardless of their rate of generation.

A slight dependence on  $\Delta$  was observed, with a 20% increase in noise being recorded as the correlation (delay) interval increased from 10  $\mu$ s to 25  $\mu$ s. No significant change in  $N_o$  was observed as the enabling time was varied from 35  $\mu$ s to 175  $\mu$ s. These correspond to the switching on of the MOSFET 15 to 155  $\mu$ s before the first (reference) sampling action.

## 5 CONCLUSIONS AND RECOMMENDATIONS

This series of experiments has established that both p-channel and n-channel enhancement-mode MOSFETs can be rapidly switched on and off at temperatures as low as 2.8 K so that switch-sampled readout of a VLWIR Ge:Ga focal plane is electronically feasible. Furthermore, the data demonstrate that noise levels as low as 100 rms electrons per sample (independent of sample rate) can be achieved, using existing p-channel MOSFETs, at overall rates up to 30,000 samples/second per multiplexed channel (e.g., 32 detectors at a rate of almost 1,000 frames/second). Run-of-the-mill devices, including very-low-power-dissipation n-channel FETs, would still permit noise levels of the order of 500 electrons/sample.

Aerojet recommends that the next step in the development of this technology should be fabrication and evaluation of a prototype cryogenic system of limited size--say four Ge:Ga detectors with associated cryoFET readout, assembled as a chip and wire hybrid. The development of a single-channel prototype CDS circuit specifically designed to handle the transients peculiar to the switch-sampled mode of operation would also be useful. Ultimately, it is expected that, for very large scale arrays, it will be appropriate to develop special-purpose monolithic silicon-MOS readout chips with which detector arrays may be hybridized using "indium bump" technology.